ABSTRACT

A system and method that converts a series of input data words at a first data width to a series of output data words at a smaller data width. In order to achieve 10-Gigabit Ethernet over an optical network, data must be converted from 66-bit words to 64-bit words (the smaller data width) at a faster clock rate, such that the concatenation of the series of input data is equivalent to the concatenation of the series of output data. This is accomplished by shifting the input data such that it is either prefixed by zeros, suffixed by zeros, or both, depending on the stage of the progression of the series. The shifted data is then split up, with a portion of the data going into a delay register and another portion of the data either being output directly or combined with data previously stored in the delay register.